Claims

[c1] What is claimed is:

1. A management system for a dynamic random access memory (DRAM) module socket, the management system comprising:

a basic input/output system (BIOS) for storing an access control program and outputting a control signal when the access control program is activated;

a chipset comprising a pair of general purpose input/output (GPIO) terminals and a pair of access control mode output ports, the chipset connected to the BIOS for receiving the control signal and correspondingly outputting a first control output and a second control output respectively via the GPIO terminals, and outputting a first access control signal and a second access control signal respectively via the access control mode output ports;

a dynamic random access memory (DRAM) module socket comprising three access control mode input ports; and

a pair of switches for respectively receiving the first access control signal and the second access control signal and selectively outputting the first access control signal and the second access control signal to the three access control mode input ports respectively according to the first control output and the second control output.

[c2] 2. The management system of claim 1, wherein the chipset is an integrated chipset.

[c3] 3. The management system of claim 1, wherein the pair of access control mode output ports are an Error Correction Code (ECC)/Clock Enable (CKE) mode output port and a Data Input Output Mask (DQM)/CKE mode output port.

[c4] 4. The managing system of claim 1, wherein the DRAM module socket is a DDRDRAM socket.

[c5] 5. The managing system of claim 1, wherein the DRAM module socket is a RDRAM socket.

[c6] 6. The managing system of claim 1, wherein the three access control mode input ports are an ECC mode input port, a CKE mode input port and a DQM

mode input port.

[c7] 7. The managing system of claim 1, wherein the switches respectively receive the first control output and the second control output to selectively output the first access control signal and the second access control to two of the three access control mode input ports.